

09/762981

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Form PTO-1449 (Modified)	ATTY DOCKET NO. B-4089PCT 618533-7	U.S. SERIAL NO. Not yet assigned
LIST OF PATENTS AND PUBLICATIONS STATEMENT	INTERNATIONAL APPLICATION NO. PCT/GB00/02320	INTERNATIONAL FILING DATE 15 June 2000
	APPLICANT(S) Andrea Olgiati, et al.	
	FILING DATE Concurrently herewith	GROUP Not yet assigned

February 14, 2001

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	ISSUE Date	Name	Class	Subclass	Filing Date if Appropriate
TM	5,708,830	1/13/1998	Stein			9/15/1992
TM	4,589,067	5/13/1986	Porter et al.			5/27/1983
TM	5,884,050	3/16/1999	Wheeler et al.			6/21/1996
TM	4,099,236	7/4/1978	Goodman et al.			5/20/1977

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES/NO
TM	EP 0 853 283 A1	7/15/1998	EP			
TM	EP 0 581 698 A1	2/2/1994	EP			
TM	EP 0 021 365 A2	1/7/1981	EP			

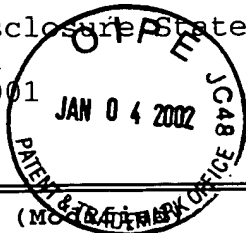
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

TM	Messias et al., "Team an array processor with a μ P for super performance in data comm," Electronic Design 8, XP-000211543, pages 115-120 (4/12/1980).

EXAMINER <i>Amia Meade</i>	DATE CONSIDERED <i>March 20, 2004</i>
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Information Disclosure Statement
 USSN 09/762,981
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Form PTO-1449 (M)	ATTY DOCKET NO. B-4089PCT 618533-7	U.S. SERIAL NO. 09/762,981
LIST OF PATENTS AND PUBLICATIONS STATEMENT	INTERNATIONAL APPLICATION NO. PCT/GB00/02320	INTERNATIONAL FILING DATE June 15, 2000
	APPLICANT(S) Andrea Olgiati, et al.	
	FILING DATE May 9, 2001	GROUP 2183

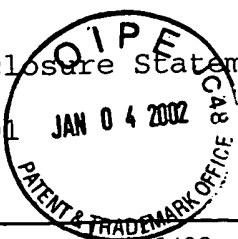
U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	ISSUE DATE	NAME	CLASS	SUB-CLASS	FILING DATE or 102(e) DATE IF APPROPRIATE
TM	5,121,498	6/92	Gilbert, et al.	395	700	
TM	5,537,620	7/96	Breternitz, Jr.	395	700	
TM	5,590,307	12/96	McClure	395	458	
TM	5,603,007	2/97	Yazdy, et al.	395	467	
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TM	5,862,385	1/99	Iitsuka	395	709	
TM	6,006,289	12/99	James, et al.	710	35	
TM	6,009,493	12/99	Fujiyama	711	1	
TM	6,049,839	4/00	Fujii, et al.	710	1	
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TM	6,209,071 B1	3/01	Barth, et al.	711	167	

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TM	0 447 145 A2	9/91	EP			
TM	0 549 924	7/93	EP			
TM	0 862 118	9/98	EP			
TM	0 924 625	6/99	EP			

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TM	2 250 615 A	6/92	GB			
TM	2-250137	10/90	JP			Abstract
TM	2-250138	10/90	JP			Abstract
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TM	98/33276	7/98	WO			
TM	98/33277	7/98	WO			

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TM	Bellows, P. and B. Hutchings, "JHDL - An HDL for Reconfigurable Systems," <i>Proceedings of the IEEE Symposium on Field-Programmable Custom Computing Machines</i> , 10 pages (April 1998).
TM	Dijkstra, E., "Co-operating Sequential Processes," <i>Programming Languages</i> , F. Genuys (ed.), pp. 43-112 (1968).
TM	Handy, J., <i>The Cache Memory Book</i> , Academic Press, pp. 9 and 12-22 (1993).
TM	Hennessy, J. and D. Patterson, <i>Computer Architecture: A Quantitative Approach</i> , Morgan Kaufman Publishers, Inc., pp. 414-416, 444-445, and 475-478 (1990).
TM	Pugh, W. and D. Wonnacott, "An Exact Method for Analysis of Value-based Array Data Dependences," <i>Languages and Compilers for Parallel Computing</i> , Springer-Verlag, pp. 546-566 (1993).

EXAMINER	DATE CONSIDERED
<i>Amia W. Hunshe</i>	<i>March 30, 2004</i>

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